LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-7. (Canceled)

8. (Original) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure; and

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region and a third doping region with the second dosage formed in the substrate adjacent to the edge of the second side of the gate structure to serve as a source region;

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

9. (Original) The device as claimed in claim 8, wherein the gate structure is composed of a gate, a gate dielectric layer, and a gate spacer.

10. (Original) The device as claimed in claim 8, wherein the first dosage is about 7.0 to 9.0E12 ions/cm^2.

11. (Original) The device as claimed in claim 10, wherein the second dosage is about 2.0 to 4.0E15 ions/cm^2.

12-23. (Cancelled)

24. (Previously presented) A high-voltage MOS transistor comprising:

a first drain region with a first dosage formed in a substrate, wherein the first drain region extends horizontally from a first point proximate to an upper surface of the substrate to a second point proximate to the upper surface;

a gate structure overlying the substrate and covering a portion of the first drain region extending from the first point to a third point of the first drain region located between the first and second points;

a spacer in contact with the gate structure and covering a portion of the first drain region from the third point to a fourth point of the first drain region located between the third and second points;

a second drain region with a second dosage formed within the first drain region, wherein the second drain region extends substantially from the fourth point to a fifth point of the first drain region located between the fourth and second points, and wherein the portion of the first drain region extending from the fifth point to the second point is at substantially the same horizontal level in the substrate as the first point; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.

25. (Previously presented) The high-voltage MOS transistor of claim 24 further comprising a field oxide layer substantially abutting the first doped region at the second point.

26. (Previously presented) The high-voltage MOS transistor of claim 24, wherein the first drain region has a doping concentration of approximately 7.0 to 9.0E12 ions/cm^2.

27. (Previously presented) The high-voltage MOS transistor of claim 24, wherein the second drain region has a doping concentration of approximately 2.0 to 4.0E15 ions/cm^2.

28. (Previously presented) A high-voltage MOS transistor comprising:

a first drain region formed in a substrate;

a gate structure overlying the substrate and covering a first portion of the first drain region;

a spacer in contact with the gate structure and covering a second portion of the first drain region adjacent to the first portion;

a second drain region formed within the first drain region, wherein the second drain region extends substantially from the second portion in the direction opposite the gate structure and spacer, wherein the portion of the first drain region extending beyond the second drain region is at substantially the same horizontal level in the substrate as the first portion; and

a source region formed in a substrate on the opposite side of the gate structure from the first drain region, wherein a channel region formed in the substrate between the first drain region and source region has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region.